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A Low Power, Glitch Free Programmable Divider in 0.18µm CMOS Technology

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ABSTRACT: A low power programmable frequency divider is proposed in this paper which is appropriate for WLAN applications. Multi- modulus architecture in dynamic logic with the minimum number of transistors is designed in 0.18µm CMOS technology. By using mixer, bandpass filter and switches, the divide ratios improved to 18. A technique is implemented in the dynamic 2-3 programmable divider cell for decreasing the glitches which leads to low power consumption. Based on simulation results it works up to 5GHz, with the average power about 37nW. Under a supply voltage of 1.8V, the total chip area of the multi- modulus programmable divider is 3100µm^2.

***Keywords*:** 2-3 Programmable divider cell, Divide ratio, Glitchless, Multi- modulus, Low power consumption.

INTRODUCTION

Programmable frequency divider is one of the main and basic building blocks which has an important role in frequency synthesizer for the purpose of stability, spectrum purity and frequency range in the developing of computers, global systems, mobile communication, digital TV, GPS, radar and telecontrol measures (Zhiqiang et al., 2010; Kim et al., 2011). In addition, frequency divider is an integral part of the PLL taking the input frequency from the VCO and generating one or more high quality frequencies which is appropriate for analog front- end circuits (Zhiqiang et al., 2010; Sleiman et al., 2008). Therefore the design of frequency divider is critical and tricky in order to reach the advantages of high speed, high sensitivity, low power consumption and better programmability (Sleiman et al., 2008; Lin et al., 2009; Francesco et al., 2008).

In general frequency divider categorize into two groups, analog and digital (Ching et al,. 2009). Regenerative frequency divider and the injection locking frequency divider (ILFD) belong to the analog frequency dividers while the static and dynamic logic dividers are included in digital frequency dividers. Since the dynamic logic has benefits of high speed and programmability, it is more common in the application of communication systems (Ting et al,. 2010).

In the past years, several programmable frequency dividers with various architectures have been proposed in different literatures. A current mode logic (CML) frequency dividers used in the frequency synthesizer, if having wide locking range and robust operation, consume more power and more chip area (Joonhee et al., 2011; Sun and Li, 2011). For the purpose of gaining low power consumption, smaller silicon area and larger output swing injection-locked frequency dividers have been presented, but due to the limitation of their locking and division range, they can't be practical in modern technology (Xiaopeng et al,. 2008). Also pulse- swallow programmable frequency dividers provide ultra- low power consumption, but because of some major drawbacks like complexity, limitation in their speed, high hardware and silicon area and the lack of modularity, a new TSPC divide-by-2/3 is proposed in this paper. Based on the lower number of transistors employed in this architecture, the power consumption and also chip area are decreased significantly. A design of triple- mode programmable frequency divider due to the switching technique is improved in this circuit in order to widen the range of frequency divider.

In this paper, a design of TSPC divide- by- 2/3 is proposed in section II. The topology of a multi- mode programmable frequency divider is described in section III. In section IV the simulation and measurement results are presented. At the end, section V covers the conclusion of the whole design.

PROPOSED TSPC PROGRAMMABLE FREQUENCY DIVIDER

The most common architecture of dual- modulus dividers especially divide- by- 2/3 is based on using four or more D- latches and some logic gates. These blocks are employed in a cascaded chain to extend the division ratio which leads to more power consumption and an increase in the complexity of the designs (Tarek and Kaamran, 2010). For overcoming the disadvantages of the conventional topologies, the single stage divide- by- 2/3 is presented. The TSPC divide- by- 2/3 cell which consists of only 10 transistors is shown in Fig.1. This architecture is designed for the VCO input source in the range of WLAN frequencies. The control signals which activate transistors Q_1 and Q_2 can change the division ratio from 2 to 3, respectively.

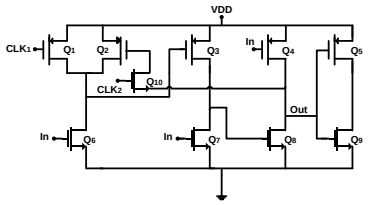

Figure 1. The TSPC divide- by- 2/3 cell

Figure 2 shows the simulation results of the two division ratios. As it is clear the glitches make the problem in the high quality operation of frequency divider in high speed.

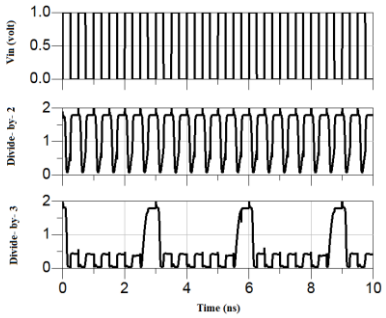

Figure 2. The divide- by- 2 and divide- by- 3 results related to V_{in}

To avoid glitches, the proposed glitch free architecture is shown in Fig. 3. The high value of resistor R_1 can decrease the voltage level and as a consequence the glitches can disappear easily in this design. Given the fact that the resistor consumes more power and increases the chip area, so the best value for it should be selected to establish a trade-off between the power consumption, chip area and the level voltage of glitches. The simulation results for the divide- by- 2/3 with the glitches resistor technique are shown in Fig. 4. Comparing with the last results it can be widely cleared that the glitches diminish in the new structure.

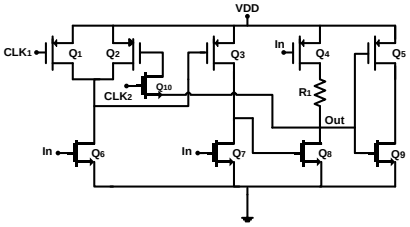

Figure 3. The proposed glitch free divide- by- 2/3 cell

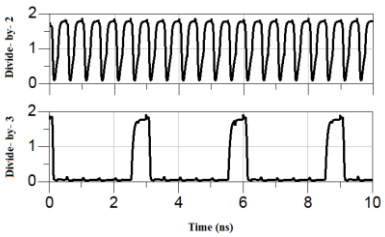

Figure 4. The divide- by- 2 and divide- by- 3 results with glitch free technique

Multi- mode programmable frequency divider

There are various architectures providing the wide range of division, such as pulse swallow dividers, cascaded dual- modulus dividers and phase rotating dividers (Hesham et al., 2011). The major drawbacks of these structures are the high power consumption and the need for extra extension logic and input buffer circuits in order to ensure correct operating of dividers with large signal swing (Sleiman et al., 2008; Nesreen and Masuri, 2009; Qinqing and Zhiqun, 2012). In this paper a multi- mode programmable frequency divider with the switching technique, one or two divide- by- 2/3 cells, a radio frequency (RF) mixer and a band- pass filter (BPF) are proposed. All the switches play an essential role in preparing the different division ratios by setting into “ON” and “OFF” states. Considering the fact that the number of divide- by- 2/3 cells is limited, not only does the power consumption remain low, but also the complexity of the extra structures like input buffer and extension logic circuit can be ignored easily. The proposed block diagram of the multi- mode programmable frequency divider is shown in Fig. 5. The mixer in this structure has two inputs to produce the output frequencies of the summation and subtraction of the two inputs. It is clear that the band- pass filter should remove the higher frequency of the summation of two inputs; therefore the output of the band- pass filter is the subtraction of two signals for the purpose of fine operating of the circuit.

For the purpose of fine operation, capacitor is used for coupling the stages. In this situation the effect of each stage on the whole circuit is diminished significantly. Although capacitors increase the chip area, play a key role in decreasing the power consumption and fining the output signal. Thus the value of the capacitor is determined based on the trade- off between the power consumption and chip area.

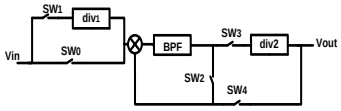

Figure 5. The proposed block diagram of the multi- mode programmable divider

The circuit of mixer and band- pass filter is proposed in Fig. 6. As it is shown in this figure the active inductor is used in this architecture to decrease the chip area while it operates in a double- balanced configuration. The mixer receives two frequencies from input stage and LO stage, then the band- pass filter passes only the subtraction of two frequencies and ignores the higher frequency from the summation of f_{in} and f_{LO} . It is important to note that the input frequency should be appropriately selected based on the operation frequency of both dividers, mixer and band- pass filter. As it is mentioned, the dividers are designed to work under WLAN frequencies, while the mixer and band- pass filter can work up to WLAN frequencies. Another crucial factor is the accurate selection of clock signals for switches in order to have the exact output of stages and consequently to reach the desired range of frequency divider from 2 to 18. Therefore the suitable combination of all blocks and switches culminates in the glitch free output signal of the programmable frequency divider.

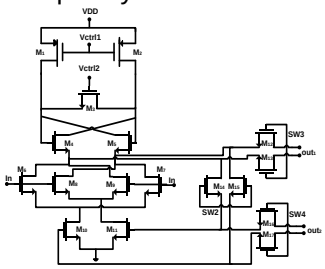

Figure 6. The proposed circuit of mixer and BPF

For the mode of 1/2 none of the divide- by- 2/3 is used from the total structure. It should be noted that it has the lowest power consumption due to the simple configuration and it is about 4nW. Therefore the programmable divider works as follows:

$$V_{in} - V_{out} = V_{out} \rightarrow V_{out} = \frac{1}{2} V_{in} \quad (1)$$

For the mode of 1/3, 1/4 and 1/6 which need only one divide- by- 2/3, the power consumption is increased up to 20nW while the function of the divider can be calculated as follows:

$$\frac{V_{in} - V_{out}}{2} = V_{out} \rightarrow V_{out} = \frac{1}{3} V_{in} \quad (2)$$

$$\frac{V_{in} - V_{out}}{3} = V_{out} \rightarrow V_{out} = \frac{1}{4} V_{in} \quad (3)$$

$$V_{in}/3 - V_{out} = V_{out} \rightarrow V_{out} = \frac{1}{6} V_{in} \quad (4)$$

For the rest of modes two divide- by- 2/3s should be worked to achieve the best operation of the programmable divider. In this case the power consumption reaches to its maximum about 37nW. The equations based on modes 1/8, 1/12 and 1/18 can be calculated as follows:

$$\frac{V_{in}/2 - 2V_{out}}{2} = V_{out} \rightarrow V_{out} = \frac{1}{8} V_{in} \quad (5)$$

$$\frac{V_{in}/2 - 3V_{out}}{3} = V_{out} \rightarrow V_{out} = \frac{1}{12} V_{in} \quad (6)$$

$$\frac{V_{in}/3 - 3V_{out}}{3} = V_{out} \rightarrow V_{out} = \frac{1}{18} V_{in} \quad (7)$$

Table 1 summarizes the different states of switches and dividers for the various modes of the frequency divider. It is absolutely certain that with the help of simple switches, the several ranges of frequencies can be produced without any need of sophisticated topologies in previous literatures.

Table 1. The state of switches and dividers for each mode

Mode	"ON" Switches	div1	div2
2	SW0, SW2, SW4		
3	SW0, SW3, SW4		2
4	SW0, SW3, SW4		3
6	SW1, SW2	3	
8	SW1, SW2, SW3	2	2
12	SW1, SW2, SW3	2	3
18	SW1, SW2, SW3	3	3

RESULTS

A simulation of the WLAN frequency divider has been realized in 0.18µm CMOS technology. The implemented division ratios are improved in to 2-18 frequency modes under 1.8V power supply. The figure of merit of the multi-modulus programmable frequency divider based on the definitions of maximum input frequency (fmax) in GHz, voltage supply (VDD) in volt and the average power consumption (P) in mW can be expressed as follows:

$$\eta = f_{max}/(P.VDD) = 75 \times 10^3 \quad (8)$$

As the main operation of this design is based on the variation of control signals of divide- by- 2/3 cells and the state of switches, the input frequency, the control signals and the output frequency are shown in Fig. 8. It is vividly shown that by changing the control signal the division ratio changes from two to three.

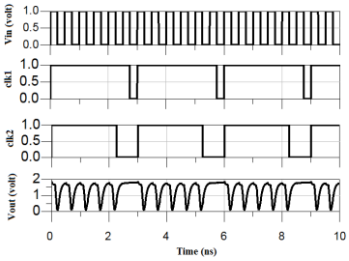

Figure 8. Input, control signals and output voltages

Thanks to the one stage of the proposed structure instead of using four D- latches in the conventional divide-by- 2/3, the power consumption measures as low as 4nW and for the high division ratios with switching technique topology reaches to 37nW. Figure 9 shows the power consumption proportional to the operating frequencies for the multi- modulus divider; as a result of low number of transistors it is much lower than the conventional architectures.

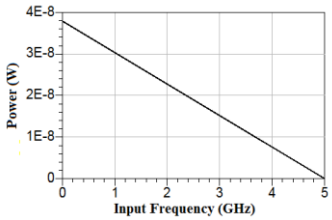

Figure 9. Power consumption versus input frequency

The layout of the proposed programmable divider is shown in Fig. 10. Comparing with the conventional divider with four D- latches, it consumes 3080µm2 which is much less than the previous structures. Table 2 demonstrates the comparison between the proposed design and some conventional circuits published recently. It goes without saying that the presented multi- stage programmable divider has the lowest power consumption with the minimum chip area in the same technology as the other literatures.

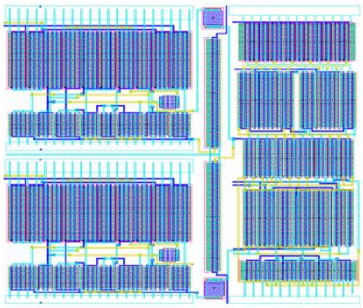

Figure 10. The layout of the proposed divider

Table 2. Characteristics comparison

	Dividing ratio	Supply voltage (v)	Power consumption	F_{max} (GHz)	Chip area	Technology (µm CMOS)
[1]	120- 400	1.8	-	2.2	-	0.18
[2]	13- 1278	1.5	3.23 mW	3.5	0.0408 mm^2	0.18
[3]	8- 255	1.8	11 mW	7.55	6630 μm^2	0.18
[7]	2- 3	1.8	3.24 mW	5.8	2000 μm^2	0.18
[9]	2403- 2480	1.8	7.7 mW	6.5	0.02 mm^2	0.18
[10]	8- 9	1	0.29 mW	6	400 μm^2	0.18
[13]	15- 16	1.8	0.7 mW	3.4	-	0.18
[14]	720- 960	1.8	3.24 mW	3	5400 μm^2	0.18
This work	2- 18	1.8	37nW	5	3100 μm^2	0.18

CONCULSION

A dynamic logic multi- modulus frequency divider in 0.18µm CMOS technology proposed in this paper. The glitch free technique with the help of implemented resistor is used to decrease the output voltage level in order to

diminish the glitches. Due to the improved switching technique, the multi- mode of divider is simply designed in order to gain low power consumption about 37nW with the minimum chip area of 3100µm2. The input operating frequency is up to 5GHz under 1.8V supply voltage.

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